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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/395,294	09/13/1999	SOPHIE WILSON	1073/OG117	5796

26111 7590 04/16/2004

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EXAMINER	
MEONSKE, TONIA L	

ART UNIT	PAPER NUMBER
2183	26

DATE MAILED: 04/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/395,296	WILSON, SOPHIE	
	Examiner	Art Unit	
	Tonia L Meonske	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *17-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *17-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 17, 18, 19, 20, 24, 25 are rejected under 35 U.S.C. 102(b) as being clearly anticiapted by Shiell et al., US Patent 6,317,820, cited in the prior office action, paper number 6, mailed on January 15, 2002.

3. Referring to claim 17, Shiell et al. have taught a system to process instruction sequences all having the same predetermined sequence bit length (column 3, lines 5-15), the system comprising:

a. a decode unit to decode an instruction of an instruction sequence received during an instruction fetch (Figure 1, element 115, abstract, column 3, lines 5-15, column 4, lines 1-9, column 2, lines 52-55), wherein all instructions of the instruction sequence have the same predetermined instruction bit length (column 3, lines 63-67, VLIW instructions inherently have the same predetermined instruction bit length); and

b. first and second processing channels (column 3, lines 54-58, A side and B side), each processing channel including a plurality of functional units, at least one of the functional units of each processing channel being a data processing unit (column 3, lines 56-61, S, L, and M units) and at least one other of the functional units of each processing channel being a memory access unit (column 3, lines 56-61, D unit);

c. wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations and to control the first and second processing channels based on the determination (column 2, lines 23-56).

4. Referring to claim 18, Shiell et al. have taught the system according to claim 17, as described above, and wherein, when the decode unit determines that the instruction defines two independent operations (column 2, lines 23-56, Second mode), the decode unit is operable to control the first channel to implement one of the two independent operations (column 2, lines 23-56, A side operation) and the second channel to implement the other of the two independent operations (column 2, lines 23-56, B side operation), an wherein the first and second channels execute their respective independent operations simultaneously (column 2, lines 23-56).

5. Referring to claim 19, Shiell et al. have taught the system according to claim 17, as described above, and wherein, when the decode unit determines that the instruction defines a single operation, the decode unit is operable to control the first and second processing channels to cooperate to execute the single operation (column 2, lines 23-56, First mode).

6. Referring to claim 20, Shiell et al. have taught the system according to claim 17, as described above, andwherein the first and second processing channels share at least one common register file and are capable of simultaneously accessing the at least one common register file (column 4, lines 24-34, Figure 1, elements 140a and 140b).

7. Claim 24 has nothing over claim 17 and is therefore rejected for the same reasons as set forth in claim 17.

8. Claim 25 has nothing over claim 21 and is therefore rejected for the same reasons as set forth in claim 21.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 21, 22, 23, 26, 27, and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, cited in the prior office action, paper number 6, mailed on January 15, 2002, in view of Yoshida, US Patent 5, 761,470, cited in a prior office action, paper number 16, mailed on April 3, 2003.

11. Referring to claim 21, Shiell et al. have taught the system according to claim 17, as described above. Shiell et al. have not specifically taught wherein the decode unit is operable to determine whether the instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction. Yoshida has taught wherein a decode unit is operable to determine whether an instruction defines a single operation or two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction (Figure 25, elements 505 and 506). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Shiell et al. make said determination based on at least one identification bit in at least one predetermined bit location, as taught by Yoshida, in order to easily determine whether the bit length defines a single operation or two independent operations. Having the designated bits at predetermined bit locations in the instruction itself would eliminate the need to have a separate instruction (Shiell

et al., column 2, lines 53-55) preceding the instruction in order to set up the channels for execution.

12. Referring to claim 22, Shiell et al. have taught the system according to claim 21, as described above, and wherein, when the instruction has a length of n bits (Yoshida, Figure 25, element 501s and 502), the predetermined bit locations include the n/2th bit (Yoshida, Figure 25, element 506, counting from right to left of the bits in instruction 501) and the nth bit (Yoshida, Figure 25, element 505, counting from right to left of the bits in instruction 501).

13. Referring to claim 23, Shiell et al. have taught the system according to claim 21, as described above, and wherein the decode unit is operable to identify certain combinations of the two independent operations based on the at least one identification bit, and wherein

a. a first combination denotes two data processing operations (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A and an instruction from side B are dispatched to either the S, L, or M functional units.),

b. a second combination denotes two memory access operations (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A and an instruction from side B are dispatched to the D functional units.),

c. a third combination denotes a data processing operation and a memory access operation (Column 2, lines 23-56, column 3, line 50-column 4, line 9, Second Mode, This combination is identified when an instruction from side A is dispatched to either the S, L, or M functional unit and when an instruction from side B is dispatched to the D functional unit.), and

d. a fourth combination denotes a long instruction (Column 2, lines 23-56, column 3, line 50-column 4, line 9, An instruction dispatched in the First Mode.).

14. Claim 26 has nothing over claim 21 and is therefore rejected for the same reasons as set forth in claim 21.

15. Claim 27 has nothing over claim 6 and are therefore rejected for the same reasons as set forth in claim 6.

16. Claim 32 has nothing over claims 17-31 and is therefore rejected for the same reasons as set forth in claims 17-31.

17. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, cited in the prior office action, paper number 6, mailed on January 15, 2002, in view of Panesar, US Patent 6,697,774.

18. Referring to claim 28, Shiell et al. have taught the limitations of the claim, as described above in the rejection to claim 17. Shiell et al. have not specifically taught that the processor based system is implemented with commands. However, Panesar has taught that the simulation of a processor, with commands such as VHDL, is necessary prior to implementing a circuit in silicon to establish how a device will actually operate (Panesar, column 8, lines 25-36). It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the processor-based system with commands, as taught by Panesar, as it is necessary prior to implementing a circuit in silicon for the desirable purpose of determining how the processor will operate (Panesar, column 8, lines 25-36).

19. Claims 29, 30, 31, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shiell et al., US Patent 6,317,820, cited in the prior office action, paper number 6, mailed on January 15, 2002, in view of Yoshida, US Patent 5, 761,470, cited in a prior office action, paper number 16, mailed on April 3, 2003, and Panesar, US Patent 6,697,774.

20. Referring to claim 29, Shiell et al. in combination with Panesar have taught the article according to claim 28, as described above. Shiell et al. in combination with Panesar have not specifically taught wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on at least one identification bit at at least one predetermined bit location in the instruction. However, Yoshida has taught (Figure 25, elements 505 and 506). It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the instructions of Shiell et al. make said determination based on at least one identification bit in at least one predetermined bit location, as taught by Yoshida, in order to easily determine whether the bit length defines a single operation or two independent operations. Having the designated bits at predetermined bit locations in the instruction itself would eliminate the need to have a separate instruction (Shiell et al., column 2, lines 53-55) preceding the instruction in order to set up the channels for execution. Further more it is obvious to implement this processor with commands, as taught by Panesar, as described above in claim 28.

21. Referring to claim 30, Shiell et al. in combination with Panesar and Yoshida have taught he article according to claim 29, as described above, and wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on the at least one identification bit that indicates the nature of the two independent operations when the instruction defines the two independent operations (Yoshida, Figure 25, elements 505 and 506).

22. Referring to claim 31 Shiell et al. in combination with Panesar and Yoshida have taught the article according to claim 29, as described above, and wherein the commands to enable the processor-based system to decode the instruction include the commands to enable the processor-based system to decode the instruction to determine whether the instruction defines the single operation or the two independent operations based on an n/2th bit (Yoshida, Figure 25, element 506, counting from right to left of the bits in instruction 501) and an nth bit of the instruction (Yoshida, Figure 25, element 505, counting from right to left of the bits in instruction 501) having n bits (Yoshida, Figure 25, element 501 and 502).

23. Claim 33 has nothing over claims 17-31 and is therefore rejected for the same reasons as set forth in claims 17-31.

Response to Arguments

24. On page 9, Applicant argues in essence:

> *"The examiner relies on col. 2, lines 23-56 of Shiell to allegedly show that Shiell teaches a decode unit that is operable to detect for each instruction for each instruction having a predetermined bit length whether the instruction defines a single operation or two independent operations and to control the first and second channels in dependence on the detection. Applicant, however, contends that the cited art merely shows that in the second mode, the data processor can process two independent program instruction streams simultaneously."*
>
> Applicant is correct in that in the second mode the data processor can process two independent program instruction streams simultaneously. However, Shiell et al. have in fact taught that the data processor is changed from the first mode to the second mode via an instruction. The instruction must inherently be decoded by a decode unit in order to switch modes via the instruction. Therefore this argument is moot.

25. On page 9, Applicant argues in essence:

"Shiell does not even suggest that an instruction within the instruction sequence can include more than one operation. Moreover, Shiell does not even suggest that the instruction stream has a predetermined bit length."

However, Shiell has taught an instruction within the instruction sequence that includes more than one operation (Shiell et al., Column 3, lines 60-67, VLIW instructions have multiple operations.). Furthermore, Shiell et al. have in fact taught an instruction stream with a predetermined bit length (Column 3, lines 5-15). Therefore this argument is moot.

26. On page 9, Applicant argues in essence:

"Shiell fails to teach or suggest a system to process instruction sequences all having the same predetermined sequence bit length, wherein the system includes a decode unit that is operable to determine whether an instruction of the instruction sequence defines a single operation or two independent operations and to control the first and second processing channels based on the determination. ... Yoshida fails to remedy the failure of Shiell..."

However, Shiell et al. have in fact taught above said limitations. Please see the rejection to claim 17 above. Therefore this argument is moot.

Conclusion

27. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tonia L Meonske whose telephone number is (703) 305-3993. The examiner can normally be reached on Monday-Friday, 9-6:30, with every other Friday off.

28. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

29. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tlm

RICHARD L. ELLIS
PRIMARY EXAMINER